CLAIMS

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1. A ladder circuit editing system for inputting and editing a sequence program for a program controller in the form of a ladder diagram, said ladder circuit editing system having an unavailable area in which at least one circuit pattern that has been input is stored and an available area in which a new circuit pattern is stored, and successively inputting circuit patterns from said available area, said ladder circuit editing system comprising:

a circuit pattern extracting means for comparing a circuit element contained in a circuit pattern being stored in said available area with a circuit element contained in a circuit pattern stored in said unavailable area, and extracting a circuit pattern that contains a circuit element agreeing with a stored one;

a display means for displaying the circuit pattern extracted by said circuit pattern extracting means on an input screen; and

a copying means for copying the circuit pattern extracted by said circuit pattern extracting means into said available area according to an operator's entry.

2. A ladder circuit editing system according to Claim 1, wherein said display means successively displays a plurality of circuit patterns extracted by said circuit pattern

extracting means, and said copying means copies any circuit pattern, which is selected based on the operator's entry from among the plurality of successively displayed circuit patterns, into said available area.

3. A ladder circuit editing system according to claim 2, wherein said display means displays a previously selected circuit pattern as a top priority.

4. A ladder circuit editing system according to claim 3, further comprising a selected circuit pattern address storage area in which the address of a previously selected circuit pattern is stored, and a replacing means for placing the address of a selected circuit pattern at the head of said selected circuit pattern address storage area, wherein said display means displays as a top priority the previously selected circuit pattern according to the order of addresses stored in said selected circuit pattern address storage area.